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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,554	03/12/2001	Donald Henry Willis	PU010053	1285

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EXAMINER

NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/804,554

Applicant(s)

WILLIS, DONALD HENRY

Examiner

Paulos M. Natnael

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-17, 20, 21, 23-26, 29, 32 and 33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4, 6-13 and 32 is/are allowed.
- 6) ☒ Claim(s) 14-17, 20, 21, 23-26, 29 and 33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
2. Claims **23-26 and 29** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **23**, line 2, the claimed "said input signal" lacks antecedent basis.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
4. Claims **14-17, 20, 21 and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. U.S. Pat. No. 5,111,297.

Considering claim **14**,

a) a delay memory for delaying said input video signal to provide a first video signal delayed with respect to said input video signal, is met by Second Frame Memory 22, Fig.6;

b) a first speed up memory for receiving said input video signal, is met by first frame memory 21, Fig.6, which is capable of reading twice as fast (i.e., speed-up).

c) a second speed up memory coupled to an output of said delay memory for speeding up said first video signal, is met by Line Memory 23, fig.6; (see col. 7, lines 1-17)

d) means for simultaneously supplying said first and second video signals to separated areas of a display, said means comprising a multiplexer coupled to said first and second speed up memories, is met by second selection circuit 26, fig.6 which supplies the selected pictures to the display (or the picture-in-picture double-scanning television receiver) a main signal and a sub picture signal from the output of the first frame memory or the output of the first selection circuit through the line memory. (Note that Tsuji discloses first and second main picture signals and first and second sub picture signals).

Tsuji does not specifically use the term simultaneously.

However, the examiner submits that it is notoriously well-known in the art that the PIP video signal and the Main video signal can simultaneously be displayed on the

display screen of the television receiver. The PIP of course is overlaid on the main signal, yet, given a reasonably broad interpretation, separated from each other. It would have been therefore obvious to the skilled in the art at the time the invention was made to readily recognize and implement the teaching of Tsuji according to the discussion as shown above.

Considering claim **15**, the frame rate multiplier of claim 14, wherein said delay memory comprises a partial frame memory storing one frame of said video signal;

Regarding claim **15**, Tsuji does not specify how large the memories are. However, it would have been obvious matter of design choice to modify the Tsuji reference by having a first memory that is $\frac{1}{2}$ of a frame or $\frac{2}{3}$, $\frac{3}{4}$ or, $\frac{4}{5}$ of a frame, etc. since applicant has not disclosed that having such size difference solve any stated problem or is for any particular purpose and it appears that any other memory would perform equally well.

Considering claim **16**, the frame rate multiplier of claim 14, wherein said speed up memory comprises an array of speed up memories, is met by the Second Frame memory 22, fig.6;

Considering Claim **17**, the frame rate multiplier of claim 14, wherein said delay memory comprises an array of memories, is met by line memory 23, fig.6, which is coupled to

Frame Memory 22 and “produces an output signal which is the interpolated scanning line video signal b of the previous line.” (col. 6, lines 8-9)

Considering claim **20**, the frame rate multiplier of claim 14, wherein said delay memory and said first speed up memory comprise a single memory;

Regarding claim 20, making separate item integral by functionally combining them is not patentable. (See *In re Larson*, 144 USPQ 347 (CCPA 1965); see also *In Lockhart*, 90 USPQ 214 (CCPA 1951)) and it would have been obvious to those with ordinary skill in the art to modify the same by combining the two memories into one in order to make the device compact and/or less costly.

Considering Claim **21**, the frame rate multiplier of claim **14**, wherein said delay memory and said first and second speed up memories comprise a single memory.

Regarding claim **21**, see rejection of claim 20;

Considering claim **33**, the frame rate multiplier of claim **14** further comprising a controller coupled to said multiplexer such that said multiplexer is controlled to alternately select a number of successive lines from said first and second speed up memories so as to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display, is met by field polarity discriminator 12, fig.6;

Response to Arguments

5. Applicant's arguments filed April 8, 2005 have been fully considered but they are not persuasive. Applicant argues that "Nowhere would the combination suggested by the Examiner show or suggest any means for simultaneously supplying the first and second video signals to separated areas of a display, as specifically recited in claim 14.

The Examiner submits however that Tsuji et al. disclose a picture-in-picture (PIP) double-scanning television receiver comprising a selector or multiplexer that selects a main signal and a sub picture signal from the output of the first frame memory or the output of the first selection circuit through the line memory. Tsuji discloses first and second main picture signals and first and second sub-picture signals. As is well-known in the art, the sub-picture and the main picture can be displayed simultaneously on the display, on separate areas, albeit, the PIP overlaid on main picture. Note also that claim 14 does not recite LCD and, thus, the Tsuji reference meets the claim as claimed.

Allowable Subject Matter

6. Claims **1-4, 6-13, 32** are allowable over the prior art.
7. Claim **23** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
8. Claims **24-26 and 29** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method for multiplying the frame rate of an input video signal comprising the step of simultaneously delaying and speeding up said input video signal to provide a first video signal delayed with respect to said input video signal and a second video signal speeded up with respect to said input video signal; speeding up said first video signal to provide a speeded up first ' video signal; and simultaneously supplying at least a portion of said second video signal and at least a portion of said speeded up first video signal to separated areas of a liquid crystal display, as in claim 1;

Multiplying the frame rate of a video signal comprising the steps of delaying said input video signal for a time less than one a frame period to provide a first video signal delayed with respect to said input video signal; speeding up said first video signal to provide a speeded up first video signal', speeding up said input video signal, alternately supplying lines of said speeded up input video signal and lines of said speeded up first video signal; and, simultaneously writing said alternately supplied lines into separated areas of a liquid crystal display, as in claim 9;


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
May 14, 2005



PAULOS M. NATNAEL
PATENT EXAMINER